High Efficiency Wideband 6 to 18 GHz PHEMT Power Amplifier MMIC

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ABSTRACT — **Design and performance of a power amplifier that has established new benchmarks for 6 to 18 GHz power is reported. The amplifier achieved 7.5 Watts max, 5.4 Watts average, 4 Watts min with 36 % max, 22 % average PAE and 12 dB of power gain from 6 to 18 GHz. This output power, bandwidth, and efficiency is superior to the best previously reported results [1,2]. The amplifier is implemented in a fully selective 0.15 um double recess power PHEMT process.**

I. INTRODUCTION

Wideband Microwave MMIC power amplifiers are of interest to Electronic Warfare and Countermeasures due to their small size, low cost, and reliability. Individual amplifiers are combined into power modules and these power modules are utilized in expendable decoys or deployed in phased arrays. In this paper we describe the design and performance of a fully monolithic 6 to 18 GHz power amplifier that can be power combined to achieve the range of power outputs desired for these applications. A typical power module combines four MMICs with a power output in the range of > 10 Watts. Phased arrays for ECM are usually cross-polarized with two MMICs per polarization channel. For a typical array size of 64 elements the power output is > 300 Watts. Low loss spatial combining techniques [3] with several hundred MMIC elements can extend the power to > 1 KW.

II. PHEMT MMIC PROCESS

The PHEMT MMICs were fabricated using a 0.15 um double recess fully selective (etch stop) process. This process is key to achieving the results presented here, providing the high gain and current density necessary for efficient power amplification, while the etch stops result in uniformity and high yield. Figure 1 summarizes some of the key parameters of the PHEMT device. The MMIC is implemented on a 55 um thick substrate with slot vias under every source for high gain and excellent thermal properties. The MMIC incorporates 25 ohms /• TaN resistors and 400 pF/mm^2 MIM SiN capacitors.

Parameter	Mean
Peak Gm (mS/mm)	450
Vgs @ Peak Gm (Volts)	-0.15
Ids @ Peak Gm (mA/mm)	240
Idss (mA/mm)	290
Imax (mA/mm)	540
BVgd @ 1 mA/mm (Volts)	14.1

Figure 1: DC Parameters of Fully Selective 0.15 um Double Recess PHEMT.

III. CIRCUIT DESIGN

The design of the amplifier utilized small signal models, optimum load, and optimum source data. The matching networks for the amplifier (input, interstage, output) were designed considering small signal response and power transfer to the optimum source or load impedance simultaneously. A finger length of 100 um was selected for high gain [4], and models were generated for a 2 finger 200 um periphery unit cell. After examining the power gain characteristics of this PHEMT at 18 GHz, an interstage ratio of 4:1 was selected.

Prior to beginning circuit optimization, appropriate matching topologies and passive structures were selected. Recognizing that problems can arise due to inadequate bias line isolation, several decoupling structures were developed with increasing current handling capability. Gate and drain bias networks employed MIM capacitors with slot vias placed closer to the matching circuit side to maintain high isolation from 1 to 40 GHz. A high current U-shaped MIM capacitor structure was developed for the second stage drain feeds of the HPAs. This structure is able to maintain bias line isolation while passing over 2 Amps of current and not exceeding electromigration design rules. Considerable effort was expended on making sure the amplifier was stable. Some of the techniques used were: resistor terminated inductive gate matching networks, series parametric oscillation suppression

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resistors (implemented in ohmic metal), RLC feedback to reduce out-of-band gain, and odd mode resistors for odd mode stability enhancement. On wafer test resistors were incorporated into the drains (where possible) mitigating drain bias loop feedback problems. All the bias lines carrying considerable current were analyzed for voltage drop and derated for electromigration.

IV. MMIC DESCRIPTION

The two-stage MMIC HPA (Figure 2) consists of four 800 um cells driving sixteen 800 um cells for a total gate periphery of 16 mm. The matching networks for the amplifier (input, interstage, output) were designed considering small signal response and power transfer to the optimum source or load impedance simultaneously.

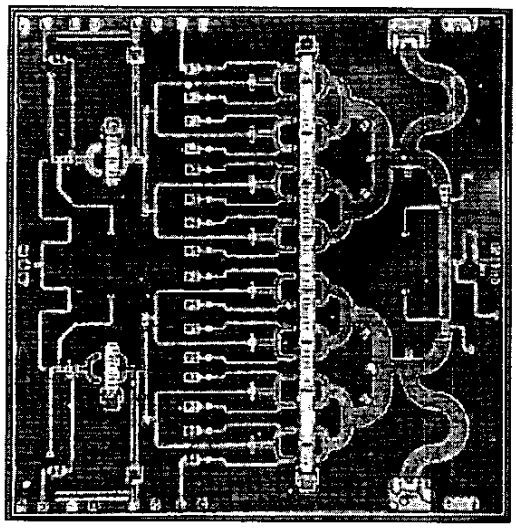

Figure 2: Photograph of 6 to 18 GHz Power Amplifier MMIC (Chip size is 5.8 mm x 5.8 mm x 55 um)

The first step in the design process is the design of the output matching network. Line widths are sized appropriately for current handling and constrained during the optimization. MIM capacitors are used in several places to capacitively load the transmission lines and reduce their length as well as provide some impedance transformation. The network is optimized for match to the optimum load at the device. The goal of better than a 12 dB large signal return loss across the 6 to 18 GHz band was achieved which results in less than 0.6 dB of load pull. The insertion loss of the output matching network is less than 0.9 dB.

The second step in the design process is the design of the interstage network. This network is a compromise between small signal gain and large signal power transfer. At frequencies where the drain of the first stage is poorly matched to the optimum load, the interstage must have a good gain match to insure that the output stage saturates first. This compromise is achieved by calculating the interstage margin which takes into account gain, ratio, and estimated load pull to the first stage device. In this design interstage margin is a minimum of 2 dB.

The final step in the initial design process is the design of the input network. This network provides a perfect match at 18 GHz for maximum gain and increasing mismatch towards the low end of the band to provide some gain slope compensation, since the amplifier is intended for use in a balanced configuration.

After the initial design of the three networks is complete, they are optimized to account for the non-unilateral nature of the large transistor periphery. During this process stability is analyzed and adjustments made to resistor values. Since dimensions were constrained appropriately in the design process no changes were necessary during the layout process.

V. MEASURED PERFORMANCE

The MMIC HPA was tested on-wafer with pulsed RF and DC. A pulse width of 30 usec at a duty cycle of 10 % was utilized. Figure 3 shows power output vs frequency for supply voltages of 5 to 6.5 Volts. The amplifier achieved 7.5 Watts max, 5.4 Watts average, 4 Watts min with 36 % max, 22 % average PAE and 12 dB of power gain from 6 to 18 GHz. With an output periphery of 12.8 mm an average power density of 0.43 W/mm was achieved. Compared to the best amplifiers reported, 3.4 Watts in [1] and 1.8 Watts in [2], these amplifiers achieve the highest power output and efficiency over the 6 to 18 GHz bandwidth.

The amplifiers have also been evaluated CW, attached to a CuW carrier. Compared to the on-wafer pulse data, the CW power output of the amplifiers were within 0.5 dB.

The amplifiers have been assembled into a four way combined power module that has demonstrated greater than 10 Watts.

V. CONCLUSION

We have reported on the design and performance of a power amplifier that has established new benchmarks for 6

to 18 GHz performance: 7.5 Watts max, 5.4 Watts average, 4 Watts min with 36 % max, 22 % average PAE and 12 dB of power gain from 6 to 18 GHz. This output power, bandwidth, and efficiency is superior to the best previously reported results.

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REFERENCES

[1] A. R. Barnes, M. T. Moore, M.B. Allenson, "A 6-18 GHz Broadband High Power MMIC for EW Applications," 1997 IEEE MTT-S IMS Digest, pp. 1429-1432.

[2] M. Salib, A. Gupta, D. Dawson, "A 1.8 Watt 6-18 GHz HBT MMIC Power Amplifier," IEEE MGW Letters, September 1993, pp 325-326.

[3] J. J. Sowers, D. J. Pritchard, A. E. White, W. Kong, O.S.A. Tang, D. R. Tanner, K. Jablinskey, "A 36 Watt V-Band Solid State Source," 1999 IEEE MTT-S IMS Digest, pp. 235-238.

[4] D. Teeter, High Power MMIC Amplifier Workshop, 1998 IEEE MTT-S IMS Symposium.

Figure 3: Power Output vs Frequency vs Drain Voltage (5 Volts unless specified)